CLAIMS:

1. (Currently amended) A ~~cache coherent memory system for use in a~~ non-homogeneous multiprocessor system, comprising:

a first processor coupled to a first local store;

a first cache associated with said first processor;

one of a second processor or other device non-homogeneous with said first processor; [[and]]

multiprocessor bus means connected to said first cache of said first processor and to said one of a second processor or other device non-homogeneous with said first processor for providing cache coherent communications via said bus means; and

a system memory having a coherent memory space, the system memory being shared by the first processor and the one of a second processor or other device non-homogenous with said first processor, wherein the coherent memory space in system memory includes a local store alias portion that maps a local store address space into a real address space of the system memory, and wherein the one of a second processor or other device non-homogeneous with said first processor accesses the first local store of the first processor using the local store alias portion of the coherent memory space in the system memory.

2. (Original) The apparatus of claim 1 comprising, in addition, a second cache associated with said one of a second processor or other device non-homogeneous with said first processor and connected to said bus means.

3. (Currently amended) A cache coherent multiprocessor system, comprising:

a shared memory;

a first cache;

a first processor, coupled to the first cache and the shared memory, having a first local store, wherein the first processor [[that]] normally communicates directly with said shared memory and stores retrieved data in said first cache;

a second processor, of a configuration different from said first processor, said second processor not typically communicating directly with said shared memory; and

a cache coherent system communicating with both said first and second processors, wherein the shared memory has a coherent memory space that includes a local store alias portion that maps a local store address space into a real address space of the shared memory, and wherein the second processor accesses the first local store of the first processor using the local store alias portion of the coherent memory space in the shared memory.

4. (Original) The apparatus of claim 3 comprising, in addition:

a second cache, associated with said second processor, in which data normally first obtained from shared memory is stored.

5. (Currently amended) A method of sharing the use of system memory data by heterogeneous devices in a multiprocessor system, comprising:

sending a request for a copy of system memory stored data to coherent memory configured caches of other devices, including caches of heterogeneous devices, before attempting retrieval directly from system memory;

storing data, retrieved from a cache of a heterogeneous device in a cache associated with the requesting device; and

updating a state table associated with each coherent memory configured cache to reflect the appropriate state after the data is stored in the cache of the requesting device, wherein the system memory is shared by the heterogeneous devices and has a coherent memory space that includes a local store alias portion that maps a local store address space of at least one local store associated with at least one of the heterogeneous devices into a real address space of the system memory, and wherein a first heterogeneous device accesses a local store of a second heterogeneous device using the local store alias portion of the coherent memory space in the system memory.

6. (Canceled)

7. (Currently amended) A computer program product for sharing the use of system memory data by heterogeneous devices in a multiprocessor system, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer code for sending a request for a copy of system memory stored data to coherent memory configured caches of other devices, including caches of heterogeneous devices, before attempting retrieval directly from system memory;

computer code for storing data, retrieved from a cache of a heterogeneous device, in a cache associated with the requesting device; and

computer code for updating a state table associated with each coherent memory configured cache to reflect the appropriate state after the data is stored in the cache of the requesting device, wherein the system memory is shared by the heterogeneous devices and has a coherent memory space that includes a local store alias portion that maps a local store address space of at least one local store associated with at least one of the heterogeneous devices into a real address space of the system memory, and wherein a first heterogeneous device accesses a first local store of a second heterogeneous device using the local store alias portion of the coherent memory space in the system memory.

8. (Canceled)

9. (New) The system of claim 1, wherein the one of a second processor or other device non-homogenous with the first processor is a second processor, and wherein the second processor is one of a control processor or a data plane processor.

10. (New) The system of claim 9, wherein the first processor accesses a portion of data in a second local store associated with the second processor using the local store alias portion of the coherent memory space in the system memory, and wherein the portion of data accessed in the second local store is cached in the first cache.

11. (New) The system of claim 2, wherein the second processor or other device non-homogeneous with the first processor accesses a portion of data in the first local store

using the local store alias portion of the coherent memory space in the system memory and stores the portion of data in the second cache.

12. (New) The system of claim 1, wherein data transfers between the first local store and the system memory are performed using the local store alias portion of the coherent memory space in the system memory.

13. (New) The method of claim 5, wherein the first heterogeneous device is one of a control processor or a data plane processor.

14. (New) The method of claim 5, wherein the second heterogeneous device accesses a portion of data in a second local store associated with the first heterogeneous device using the local store alias portion of the coherent memory space in the system memory, and wherein the portion of data accessed in the second local store is cached in a first cache associated with the second heterogeneous device.

15. (New) The method of claim 5, wherein the first heterogeneous device accesses a portion of data in the first local store using the local store alias portion of the coherent memory space in the system memory and stores the portion of data in a second cache associated with the first heterogeneous device.

16. (New) The method of claim 5, wherein data transfers between the first local store and the shared memory are performed using the local store alias portion of the coherent memory space in the system memory.

17. (New) The computer program product of claim 7, wherein the first heterogeneous device is one of a control processor or a data plane processor.

18. (New) The computer program product of claim 7, wherein the second heterogeneous device accesses a portion of data in a second local store associated with the first heterogeneous device using the local store alias portion of the coherent memory

space in the system memory, and wherein the portion of data accessed in the second local store is cached in a first cache associated with the second heterogeneous device.

19. (New) The computer program product of claim 7, wherein the first heterogeneous device accesses a portion of data in the first local store using the local store alias portion of the coherent memory space in the system memory and stores the portion of data in a second cache associated with the first heterogeneous device.

20. (New) The computer program product of claim 7, wherein data transfers between the first local store and the shared memory are performed using the local store alias portion of the coherent memory space in the system memory.

21. (New) A method, in a multiprocessor data processing system having a plurality of heterogeneous processors, for accessing a local store associated with a processor of the plurality of heterogeneous processors, comprising:

mapping a local store address space of a local store associated with a second processor of the plurality of heterogeneous processors into a real address space of a system memory using a local store alias portion of a coherent memory space of the system memory; and

accessing, by a first processor of the plurality of heterogeneous processors, the local store of the second processor using the local store alias portion of the coherent memory space in the system memory.

22. (New) A computer program product in a computer readable medium, wherein the computer program product comprises a computer readable program which, when executed by a multiprocessor data processing system having a plurality of heterogeneous processors, causes the computing device to:

mapping a local store address space of a local store associated with a second processor of the plurality of heterogeneous processors into a real address space of a system memory using a local store alias portion of a coherent memory space of the system memory; and

accessing, by a first processor of the plurality of heterogeneous processors, the local store of the second processor using the local store alias portion of the coherent memory space in the system memory.